## IN THE DRAWINGS

Corrected drawings are supplied herewith, each labeled as "REPLACEMENT SHEET".

## REMARKS

This responds to the Office Action mailed on April 28, 2006. Claims 1, 2, 5 and 6 are amended. Claims 1-30 are pending in this application. Applicant does not admit that the cited references are prior art and reserves the right to swear such references at a later date.

## §102 Rejection of the Claims

Claims 1-3 were rejected under 35 USC § 102(b) as being anticipated by Barker et al. (U.S. 5,617,577). Applicant respectfully traverses the rejection.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration.[1] It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*."[2]

As amended, claim 1 recites "a first processor having two or more processor elements and two or more input/output (I/O) ports coupled together by a first port ring that is within the first processor."

In the Response to Arguments section, the Office indicated the following:

> [U]nder the glossary of terms defined by Barker et al., the term PME refers to a single processor, memory and I/O capable system element or unit that forms one of the parallel processors (col. 7, lines 40-52).[3]

Therefore, the PME is limited to a SINGLE processor. The following table is provided to clarify the terms of claim 1 and Barker that are being equated by the Office.

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[1] *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991).
[2] *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).
[3] Office Action at ¶2.

| Claim 1 | Barker |
|---|---|
| a first processor | PME (Processor Memory Element) |
| two or more processor elements | a single processor |

Therefore, as amended, claim 1 includes two or more processor elements in the processor. Barker is limited to a single processor within the PME (as defined).

Further, claim 1 includes two or more I/O ports that are coupled together by a port ring that is within the processor. The Office indicated such limitation is met by the external ports 22, 23, 26 shown in Figure 2. While the PMEs of Barker include multiple external ports, Barker does not disclose that these ports are coupled together by a port ring that is within the PME (as recited by claim 1).

Accordingly, Barker does not disclose all of the claim limitations of claim 1. Applicant respectfully submits that the rejection of claim 1 under 35 U.S.C. §102 has been overcome. Claims 2-3 depend from claim 1 and distinguish the reference for at least the same reason.

## §103 Rejection of the Claims

In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.[4]

Claims 4-12 and 18-30 were rejected under 35 USC § 103(a) as being unpatentable over Barker et al. (U.S. 5,617,577) in view of Wilson (U.S. 5,557,734). Claims 13-17 were rejected under 35 USC § 103(a) as being unpatentable over Barker et al. (U.S. 5,617,577) in view of Wilson (U.S. 5,557,734) and Poplin (U.S. 2003/0063213).

[4] *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Claims 4-6

In addition to the remarks set forth above regarding claim 1 (from which claim 4 depends), Applicant respectfully submits the following remarks. Applicant respectfully submits that the Office Action did not make out a *prima facie* case of obviousness because even if combined, the cited references fail to teach or suggest all of the elements of claim 4.

Among the differences, claim 4 recites "the first processor is configured to transmit output from an image process operation to the second processor through the at least one I/O port of the port ring of the third processor based on a logical connection."

In the Response to Arguments section, the Office indicated the following:

> On column 12, lines 28-49, Barker et al. teach each PME has a plurality of input and output ports, which operate in different modes. Normal Mode—Used to transfer data between two adjacent PMEs. Circuit Switched Mode—Allows data and controls to pass through a PME. Zipper Mode—Used by the Array Controller to load or read data from the nodes in a cluster.[5]

The "Normal Mode" as describes only provides for transfer of data between two adjacent PMEs. Accordingly, such Mode does not provide a logical connection from a first processor to a second processor through a third processor. The "Circuit Switched Mode" allows data and controls to pass through a PME. However, this Mode is not sufficiently enabled within Barker. Rather, Barker references a different application (which is not published) for description of this mode:

> Circuit switched mode is disclosed in detail in the co-pending application entitled "PME Store and Forward/Circuit Switched Modes.[6]

Thus, Barker provides no description of the communications between the ports in a PME. Specifically, Barker does not disclose a port ring for connection of the ports within the processor that is used in the logical connection. Therefore, neither reference alone or in combination, disclose or suggest all of the claim limitations. Accordingly, Applicants respectfully submit that

[5] Office Action at ¶2.
[6] Barker at column 12, lines 41-44.

the rejection of claim 4 under 35 U.S.C. §103 has been overcome. Claims 5-6 depend from claim 4 and distinguish the references for at least the same reason.

Claims 7-30

Applicant respectfully submits that the Office Action did not make out a *prima facie* case of obviousness because even if combined, the cited references fail to teach or suggest all of the elements of claims 7-30. In particular, for at least the reasons set forth above regarding claims 1-6, Applicant respectfully submits that the cited references fail to teach or suggest all of the elements of claims 7-30. Accordingly, Applicants respectfully submit that the rejection of claim 7-30 under 35 U.S.C. §103 has been overcome.

## Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2103) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 28th day of June, 2006.

Amy Moriarty
Name

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Signature